IN THE CLAIMS:

1. (Currently Amended) A static random access memory device ~~cell~~, comprising:

a memory comprising an array of memory cells, each memory cell comprising:

a first and second passgate transistor;

a first and second storage node, wherein the first passgate transistor is connected between a first bit line and a first storage node, wherein a gate terminal of the first passgate transistor connects to a word line, and the second passgate transistor is connected between a second bit line and the second storage node, wherein a gate terminal of the second passgate transistor connects to the word line;

a first pull-up transistor ~~device~~, connected between a source voltage and the first storage node, wherein a gate terminal of the first pull-up transistor is connected to the second storage node;

a second pull-up transistor ~~device~~, connected between the source voltage and the second storage node, wherein a gate terminal of the second pull-up transistor is connected to the first storage node;

a first pull-down transistor, connected between the first storage node and a ground, wherein a gate terminal of the first pull-down transistor is connected to the second storage node; and

a second pull-down transistor, connected between the second storage node and the ground, wherein a gate terminal of the second pull-down transistor is connected to the first storage node;

wherein the first and second passgate transistors and the first and second pull-down transistors have first threshold voltages that are substantially the same, and wherein the first and second pull-up ~~pull-down~~ transistors have second threshold voltages that are substantially the same, and wherein the first threshold voltages are greater than the second threshold voltages.

2. (Currently Amended) The memory device ~~cell~~ of claim 1, wherein the first threshold voltages are a first voltage that is in a range of about 0.7 V to about 0.3 V and wherein the second threshold voltages are a second voltage that is about 10% lower than the first voltage ~~about 0.3 V~~.

3. (Canceled)

4. (Currently Amended) The memory device ~~cell~~ of claim 1 ~~3~~, wherein ~~the~~ each memory cell has a cell beta ratio of about 2.0 or greater ~~3.0~~.

5. ~22. (Canceled)

23. (New) The memory device of claim 1, wherein the first and second access transistors are NFETs, the first and second passgate transistors are NFETs, and wherein the first and second pull-up transistors are PFETs.

24. (New) A static random access memory device, comprising:

a memory comprising an array of memory cells, each memory cell comprising:

a first and second passgate transistor;

a first and second storage node, wherein the first passgate transistor is connected between a first bit line and a first storage node, wherein a gate terminal of the first passgate transistor connects to a word line, and the second passgate transistor is connected between a second bit line and the second storage node, wherein a gate terminal of the second passgate transistor connects to the word line;

a first pull-up transistor, connected between a source voltage and the first storage node, wherein a gate terminal of the first pull-up transistor is connected to the second storage node;

a second pull-up transistor, connected between the source voltage and the second storage node, wherein a gate terminal of the second pull-up transistor is connected to the first storage node;

a first pull-down transistor, connected between the first storage node and a ground, wherein a gate terminal of the first pull-down transistor is connected to the second storage node; and

a second pull-down transistor, connected between the second storage node and the ground, wherein a gate terminal of the second pull-down transistor is connected to the first storage node;

wherein the first and second pull-down transistors, the first and second pull-up transistors and the first and second passgate transistors all have first threshold voltages that are substantially the same, wherein the first threshold voltage is a voltage in a range of about 0.3V to about 0.7V.

25. (New) The memory device of claim 24, wherein the first and second access transistors are NFETs, the first and second passgate transistors are NFETs, and wherein the first and second pull-up transistors are PFETs.

26. (New) The memory device of claim 24, wherein each memory cell has a cell beta ratio of about 2.0 or greater.

27. (New) A static random access memory device, comprising:

a memory comprising an array of memory cells, each memory cell comprising:

a first and second passgate transistor;

a first and second storage node, wherein the first passgate transistor is connected between a first bit line and a first storage node, wherein a gate terminal of the first passgate transistor connects to a word line, and the second passgate transistor is connected between a second bit line and the second storage node, wherein a gate terminal of the second passgate transistor connects to the word line;

a first pull-up transistor, connected between a source voltage and the first storage node, wherein a gate terminal of the first pull-up transistor is connected to the second storage node;

a second pull-up transistor, connected between the source voltage and the second storage node, wherein a gate terminal of the second pull-up transistor is connected to the first storage node;

a first pull-down transistor, connected between the first storage node and a ground, wherein a gate terminal of the first pull-down transistor is connected to the second storage node; and

a second pull-down transistor, connected between the second storage node and the ground, wherein a gate terminal of the second pull-down transistor is connected to the first storage node;

wherein the first and second passgate transistors have first threshold voltages that are substantially the same, and wherein the first and second pull-up transistors and the first and second pull-down transistors have second threshold voltages that are substantially the same, and wherein the first threshold voltages are greater than the second threshold voltages.

28. (New) The memory device of claim 27, wherein the first threshold voltages are a first voltage that is in a range of about 0.7 V to about 0.3 V and wherein the second threshold voltages are a second voltage that is about 10% lower than the first voltage.

29. (New) The memory device of claim 27, wherein the first and second access transistors are NFETs, the first and second passgate transistors are NFETs, and wherein the first and second pull-up transistors are PFETs.

30. (New) The memory device of claim 27, wherein each memory cell has a cell beta ratio of about 2.0 or greater.